REMARKS

This Amendment is submitted in response to the Office Action dated March 11, 2003, having a shortened statutory period set to expire June 11, 2003. In the present Amendment, Claims 21-22 have been entered, meaning that Claims 9-22 are now pending.

In paragraph 2 of the present Office Action, Claims 9, 18 and 19 are rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,356,833 to *Maniar et al.* (*Maniar*). Next, in paragraph 4 of the present Office Action, Claims 10-14 and 20 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Maniar* in view of U.S. Patent No. 5,789,320 to *Andricacos et al.* (*Andricacos*). Finally, in paragraph 5 of the present Office Action, Claims 15-17 are rejected under 35 U.S.C. § 103(a) as unpatentable over *Maniar* to U.S. Patent No. 5,893,734 to *Jeng et al.* (*Jeng*). Those rejections are respectfully traversed, and favorable reconsideration of the claims is respectfully requested.

Applicant believes that *Maniar*, whether considered alone or in combination with the other prior art references of record, does not render Claim 9 unpatentable because the cited references do not teach or suggest the combination of features recited in Claim 9. In particular, the cited prior art references do not teach or suggest, "A method of fabricating a capacitor structure on a semiconductor substrate ... comprising ... forming a metallic bottom plate over the semiconductor substrate ..., forming a dielectric layer overlaying the bottom plate, forming over the dielectric layer a top plate having a smaller area than said bottom plate, ... and forming at least one insulating sidewall spacer placed against said perimeter of said top plate and overlaying a portion of said dielectric layer" (emphasis supplied).

With respect to this combination of features, paragraph 4 of the present Office Action cites the combination of *Maniar* and *Andricacos*. As an initial matter, Applicant believes that the combination of *Maniar* and *Andricacos* does not render Claim 9 unpatentable because that combination is improper for want of objective motivation or suggestion, as required by MPEP 2143.01. At page 3 of the present Office Action, the Examiner states, "It would have been obvious ... to modify the Maniar invention light [sic] of the teaching of Andricacos in order to

eliminate undesired interactions between conductive layers." However, the Examiner does not cite any passage of the cited references or any well-known teaching in the art in support of this assertion. Absent such objective support in the prior art, the Examiner's assertion is insufficient to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), and the rejection is overcome.

The combination of *Maniar* and *Andricacos* is also improper because the Examiner has not resolved the conflicts between the reference teachings as required by MPEP 2143.01. For example, Figure 7 of *Maniar* teaches a transistor having a gate structure including a sidewall spacer 74 overlaying a dielectric layer 63 and adjacent a nobium member 71. In contrast, Figure 15f of *Andricacos* discloses a capacitor having a sidewall spacer 21 that does not overlay any of dielectric layer 22a or either electrode 22, 22b. Despite such apparent conflicts between the reference teachings, the Examiner has not weighed the suggestive power of each reference before resolving each such conflict between reference teachings by adopting the structure most resembling that claimed by Applicant. Because the Examiner has failed to appropriately resolve conflicts between reference teachings, Applicant respectfully submits that the rejection under 35 U.S.C. § 103(a) is overcome.

The combination of *Maniar* and *Andricacos* is also improper under MPEP 2143.01 because the modification proposed by the Examiner in making this combination would render the structure disclosed by *Maniar* unsuitable for its intended purpose. In particular, in paragraph 4 of the present Office Action, the Examiner notes that *Andricacos* teaches a bottom plate formed of metal, inferring that the combination of such a metal bottom plate with the p-n-p transistor structure disclosed in Figures 7-9 of *Maniar* would be obvious. However, if the modification required by the Examiner's rejection were made to the p-n-p transistor structure (i.e., if n-well 61 were replaced with a metal plate), then *Maniar's* p-n-p transistor would be rendered inoperative and therefore unsuitable for its intended purpose (i.e., serving as a switching element). Consequently, Applicant believes that the rejection of Claim 9 under 35 U.S.C. § 103(a) is overcome.

Having now responded to each objection and rejection set forth in the present Office Action, Applicant believes all pending claims are now in condition for allowance and respectfully requests such allowance.

No additional fee is believed to be required; however, in the event any additional fees are required, please charge IBM Corporation Deposit Account No. **09-0456**.

Respectfully submitted,

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